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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,011	12/15/2003	Kenny Chang	JCLA11474	5574

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IRVINE, CA 92618

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,011	CHANG ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on January 19, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Change et al. (US Pub. 2003/0042455 A1).

In re claims 1, 4, 6, 9, and 11, Chang et al. shows (figs. 3, 4, and 6) a chip package structure, comprising; a carrier (602) having a surface with a power contact (301, 304A), a ground contact (306) and a signal contact (302) thereon, wherein the surface also has a chip bonding area (part of 306). The power contact and the ground contact are located close to the chip bonding area, since the ground contact is the chip bonding area. The signal contact is positioned further away from the chip bonding area; a chip (604) having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads thereon. Figure 4 shows that there is at least a passive component (401B) having at least two electrodes positioned on the carrier such that the electrodes are bonded to said power contact (301A) and said ground contact (306) respectively. A plurality of first conductive wires (606) with the two ends of each

conductive wire connected to one of the bonding pads of the chip and said power contact or said ground contact; at least a second conductive wire (606) with the two ends connected to one of the bonding pads of the chip and a corresponding signal contact such that the second conductive wire crosses over the passive component (612) without contacting the passive component [0026]. An insulating material (614) encloses the chip, the passive component, the first conductive wires and the second conductive wire.

In re claims 2, 3, 5, 7, 8, and 10, Chang et al. shows (fig. 6) that at least one of the first conductive wires (606) crosses over the passive component (612) while the remaining first conductive wires (not labeled) are adjacent to the passive component. The passive component is a capacitor [0024].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (US 6,429,536 B1) in view of Chang et al. in view of Hammand et al. (US 6,739,047 B2).

In re claims 1, 4, 6, 9, and 11, Liu et al. shows (figs. 1, 3, and 5) a chip package structure, comprising; a carrier (100) having a surface with a power contact (106), a

ground contact (104) and a signal contact (108) thereon, wherein the surface also has a chip bonding area (102), the power contact and the ground contact are located close to the chip bonding area but the signal contact is positioned further away from the chip bonding area; a chip (110) having an active surface and a backside such that the backside of the chip is attached to the chip bonding area of the carrier, wherein the active surface of the chip has a plurality of bonding pads (110a) thereon; at least a passive component (120) having at least two electrodes (12a, 120b) positioned on the carrier such that the electrodes are bonded to said power contact and said ground contact respectively; a plurality of first conductive wires (140, 180) with the two ends of each conductive wire connected to one of the bonding pads of the chip and said power contact or said ground contact; at least a second conductive wire (180) with the two ends connected to one of the bonding pads of the chip and a corresponding signal contact such that the second conductive wire crosses over the passive component without contacting the passive component (col. 4, lines 43-55 and fig. 5). The wires connected to the signal contacts are not shown but would cross over the passive component if illustrated in figure 1 because the wires connect to the signal traces (108 in fig.1) (col. 4, lines 42-55 refers back to figure 1). Although figure 1 is a prior art figure, the layout of the carrier is also used for the invention, the invention only differing in how the wires are connected (as shown in fig. 2). An insulating material encloses the chip, the passive component, the first conductive wires and the second conductive wire (col. 4, lines 52-55). Liu shows all of the elements of the claims except the ground contact connected to the chip bonding area. Hammond et al. shows (fig. 4) a chip

package structure comprising a chip (52) on a chip bonding area (40). The chip bonding area is also a ground plane that simultaneously provides heat dissipation and a low inductance-high speed RF connection to a motherboard (col. 4, lines 20-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the ground contact by forming the chip on the ground contact as taught by Hammond to simultaneously provide heat dissipation and a low inductance-high speed RF connection to a motherboard.

In re claims 2, 3, 5, 7, 8, and 10, Liu shows (fig. 5) that at least one of the first conductive wires (180) crosses over the passive component (120) while the remaining first conductive wires (not labeled) are adjacent to the passive component. The passive component is a capacitor (col. 3, lines 43-50).

Response to Arguments

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
April 4, 2005

TOM THOMAS
SUPERVISORY PATENT EXAMINER